Electrical Services Overview

K. Einsweiler, LBNL

Overview of pixel services from electrical viewpoint:

- Describe components and their interconnections
- Outline requirements for services

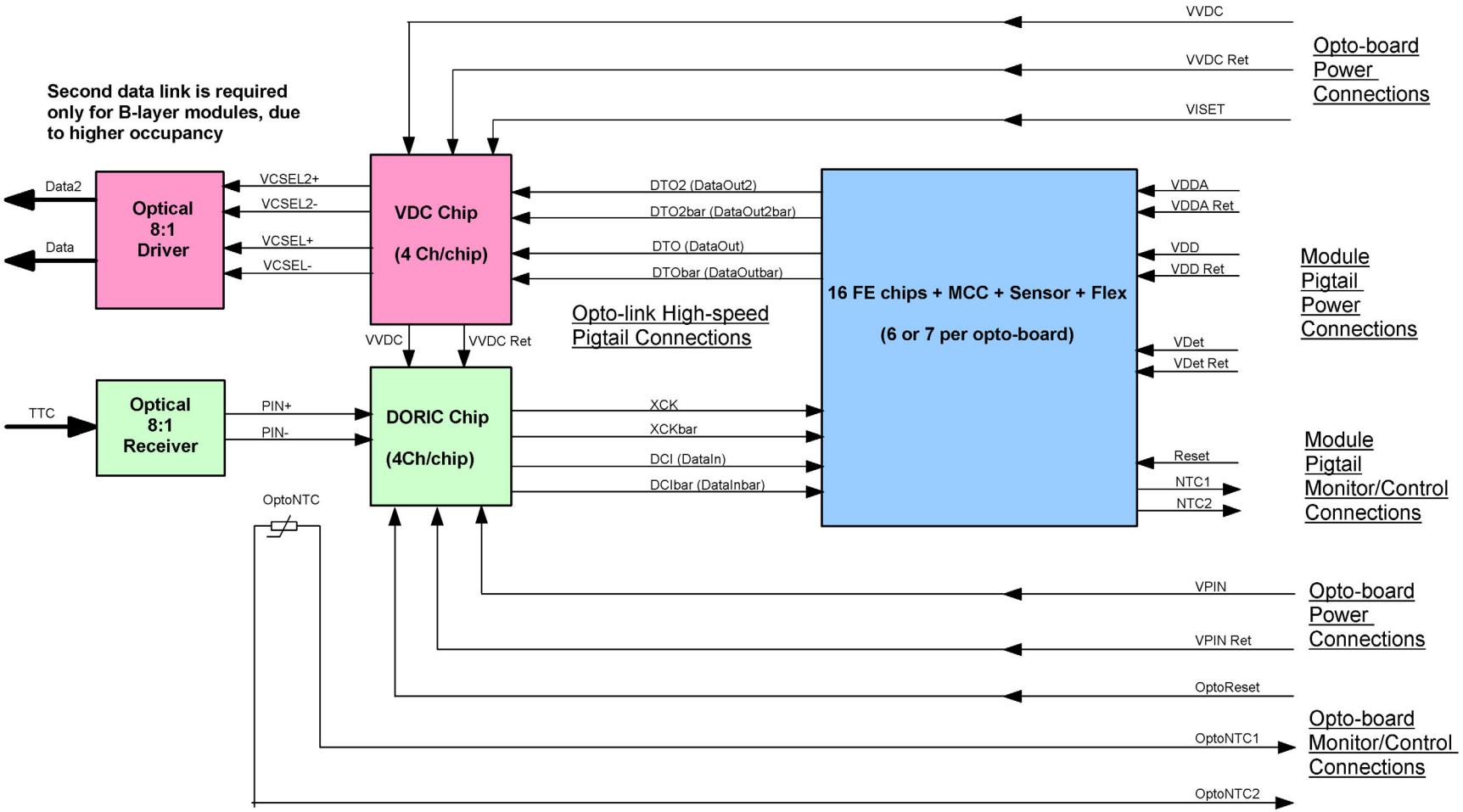
Electronics components of pixel module:

- **Front-end chip:** Sixteen 7.4x11.0mm die per module, each containing 2880 pixels of size 50μ x 400μ, plus control of internal biassing and readout circuitry.
- **Module Controller chip (MCC):** assembles data from 16 FE chips into single event, and provides module level control functions, interface to opto-electronics.
- **Power requirements:** two low voltages (one analog and one digital) and one high voltage supply per module are required. Present grounding/shielding plan calls for separate floating supplies for each module.
- **Control requirements:** one temperature monitor and one reset signal are also provided for each module. The temperature is used as part of the cooling interlock system, as well as for monitoring. The Reset is provided as a “safety net” for the MCC in case of problems during operation.

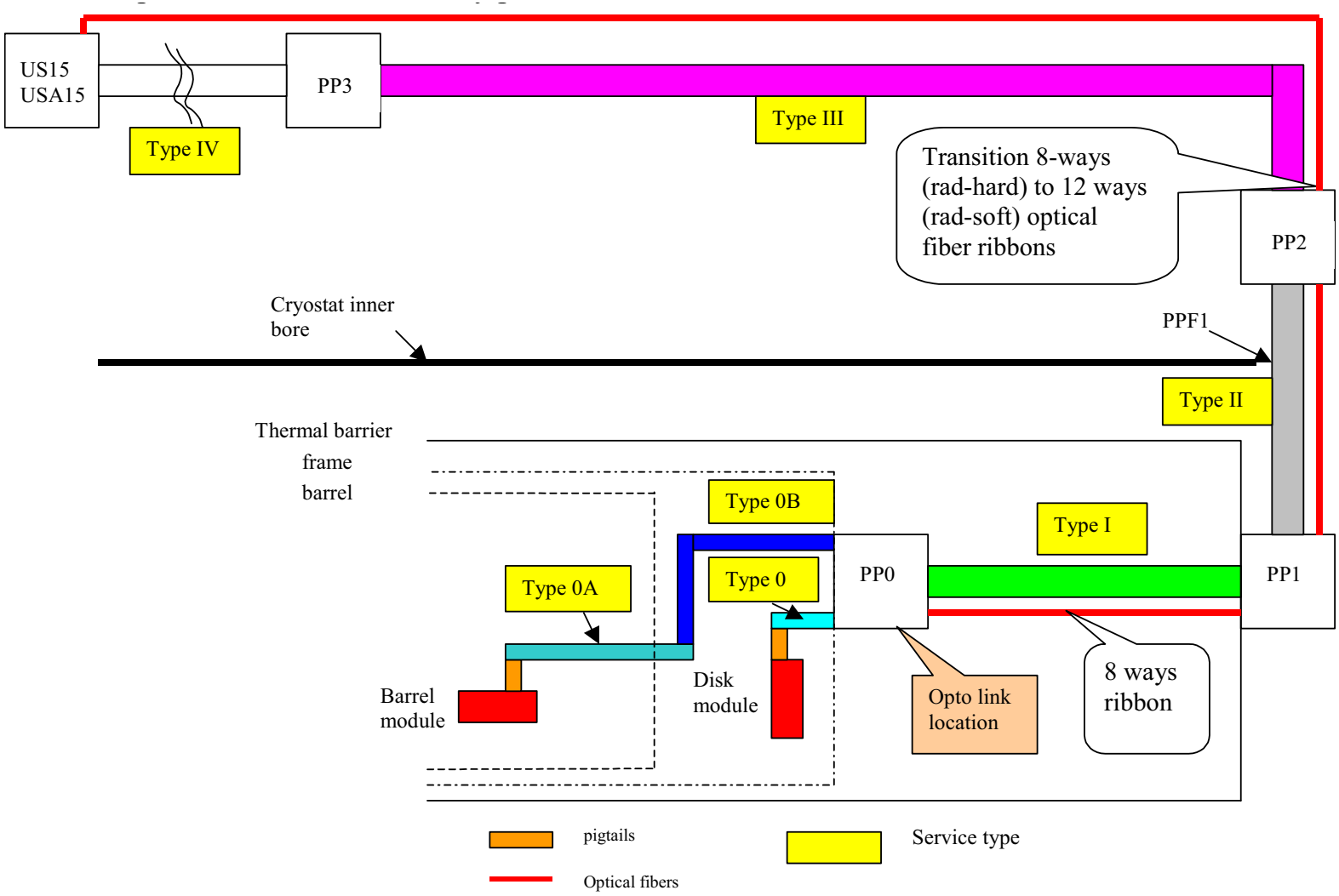
Electronics components of optical interface:

- Optical interface is implemented as a single opto-board containing opto-links for 6 or 7 modules (disk sector or half-stave). These boards are located at PP0.
- Timing and control information are sent to each module using an individual biphase-mark encoded optical stream. Data are returned from each module using 1 or 2 NRZ-encoded links which can run at either 40 or 80Mbit/s.

- **Opto-electronics:** timing and control information are decoded by DORIC chip which processes current from PIN diode. Return data are sent off-detector using a VDC chip to modulate the output of a VCSEL.
- Both chips, as well as the VCSEL, operate from a common supply. The PIN requires a separate supply. There is a separate Reset and temperate monitor.



Geography and nomenclature for services:



- PP0 contains Opto-boards. PP1 is passive.
- PP2 contains low-voltage regulators. PP3 contains DCS monitoring and interlocks.

Power distribution:

- Commercial floating power supplies are located in USA15, with a worst-case cable run of 140m from pixel detector.
- Some supplies may also be located in US15 if space and cable cost reduction require it. Preferred solution keeps all supplies in USA15.
- Power supply concept is based on “complex channels”, in which all supplies for a module (VDD, VDDA, and VDET) are collected together into a single complex channel with a common interlock.
- Modular supplies are controlled by a mainframe, which is not radiation tolerant.
- Present assumption is that two modules are operated from a single power supply to reduce channel counts. However, the service implementation brings out individual module cables to provide maximum flexibility.
- Each opto-board operates with its own independent power supplies.
- Local rad-tolerant voltage regulators are placed at PP2 (roughly 12m from modules) and operate using remote sensing to compensate for large voltage drops on low mass cable plant.
- The regulators are used for the high-current low-voltage supplies in the system (VDDA, VDD, VVDC). These are the only supplies which have significant AC currents, and hence need regulation as close to the detector as possible.
- All other supplies are quite static, and are driven directly from USA15.

Power Budget:

- Present budgets assigned to chips are based on prototypes, but not always in final technology.
- **Module budget:** is based on SPICE simulations for analog currents. Digital currents are based on earlier prototypes in 0.8μ technology. B-layer assumes 300μ pixels, with power consumption scaled proportional to channel count.

MODULE BUDGET									
	SUPPLY TYPE	*SUPPLY VOLTAGE (V)*	*SUPPLY CURRENT (mA)*	*NOMINAL VOLTAGE (V)*	*NOMINAL CURRENT (mA)*	*NOMINAL POWER (mW)*	*WORST VOLTAGE (V)*	*WORST CURRENT (mA)*	*WORST POWER (mw)*
Layer 1&2 Disks	VDDA	*8*	*1500*	*2*	*970*	*1940*	*2.5*	*1290*	*3225*
	VDD	*8*	*1000*	*2*	*500*	*1000*	*2.5*	*800*	*2000*
	VDET	*700*	*2*	*600*	*1*	*600*	*600*	*2*	*1200*
	TOTAL					***3540***			***6425***
B-LAYER									
	VDDA	*8*	*2000*	*2*	*1290*	*2580*	*2.5*	*1720*	*4300*
	VDD	*8*	*1200*	*2*	*660*	*1320*	*2.5*	*1040*	*2600*
	VDET	*700*	*2*	*600*	*1*	*600*	*600*	*2*	*1200*
	TOTAL					***4500***			***8100***

- Critical numbers for service design are worst case currents for low voltage supplies.

- **Opto-Board budget:** is based on experience with present opto-chips. Typical currents are DORIC (20mA) and VDC (20mA), with worst case DORIC (30mA) and VDC (40mA). Figures below are per module. VISET is about 1mA/module, and VPIN is negligible.

OPTO-BOARD BUDGET (7 LINKS)									
	SUPPLY TYPE	*SUPPLY VOLTAGE (V)*	*SUPPLY CURRENT (mA)*	*NOMINAL VOLTAGE (V)*	*NOMINAL CURRENT (mA)*	*NOMINAL POWER (mW)*	*WORST VOLTAGE (V)*	*WORST CURRENT (mA)*	*WORST POWER (mw)*
LAYER 1&2 DISKS	VVDC (1)	*7*	*83*	*2*	*40*	*80*	*2.5*	*70*	*175*
	VPIN	*12*	*5*	*5*	*-*		*10*	*0.06*	*1*
	VISET	*7*	*10*	*1*	*-*		*2*	*10*	*20*
	TOTAL (3)								***1246***
B-LAYER	VVDC (2)	*7*	*133*	*2*	*60*	*112*	*2.5*	*110*	*275*
	VPIN	*12*	*5*	*5*	*-*		*10*	*0.06*	*1*
	VISET	*7*	*10*	*1*	*-*		*2*	*10*	*20*
	TOTAL (3)								***1946***

- Recent agreement fixed the modularity of all opto-board supplies to be one per opto-board. In addition, due to the relatively high current of VVDC, a single sense loop is implemented from PP0 back to PP2.

Comments on using 0.25μ chips for on-detector electronics:

- Nominal maximum operating voltage for the chosen process is 2.7V. This is for reliable operation over lifetime of 10 years (100K hours).
- Maximum transient voltage is limited by multiple effects, including hot carrier effects and oxide breakdown effects. These effects can significantly shorten the lifetime, or modify the device performance for supply voltage much above 2.7V.
- The most severe issue are the breakdown and sustaining snapback voltages, above which short-channel NMOS devices can enter, and remain in, a high current, negative resistance regime, potentially leading to thermal destruction. This voltage is approximately 4.0V sustaining, and slightly higher for breakdown.
- Conservative design would ensure that chips could never see voltages close to this limit. In our services design, we have chosen worst-case round-trip voltage drops which should avoid sustained voltages above these limits. For the module voltages VDD and VDDA, have chosen worst case voltage drop from PP2 of 2V. For the opto-board voltage VVDC, have chosen worst case voltage drop of 1V.
- However, it is still possible that given the multiple time constants in our system of regulator plus long power leads, transients could appear with higher voltages. For this reason, we are also developing overvoltage protection circuits inside individual chips in the module.
- The proposed system is not conservative. Extensive system testing will be required to ensure that it is reliable and meets all pixel detector requirements.

Power Supply and Miscellaneous Connections

Supplies required at module level (supplied by pigtail):

- One HV supply to bias sensor.
- One Analog LV supply for FE chips, with remote sensing to Pigtail.
- One Digital LV supply for FE chips and MCC chip, with remote sensing to Pigtail.

Supplies required at half-stave/sector level (opto-board):

- One Digital LV supply for VDC and DORIC, with remote sensing to opto-board.
- One Analog LV supply for PIN diode bias. Very low current.
- One Analog control voltage (VISET) to adjust the VCSEL bias, low current.

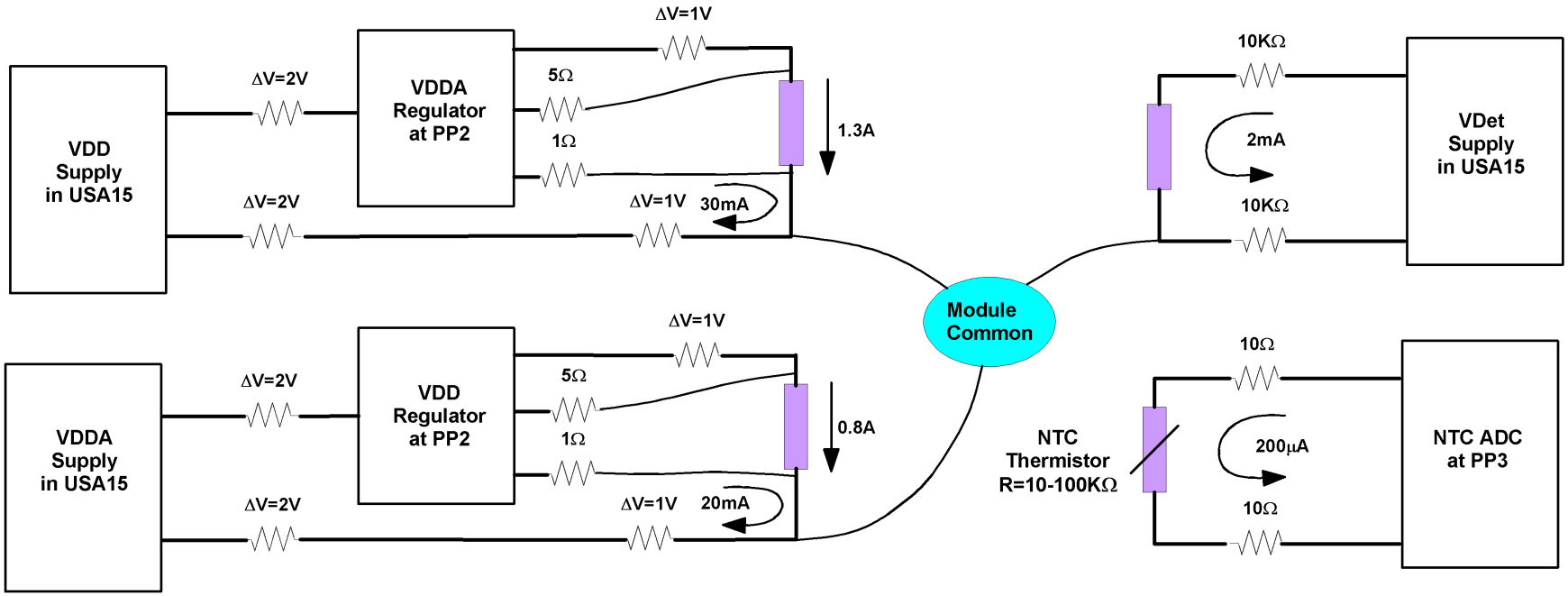
Additional DC signals in module interface:

- **Reset** is an (optional ?) slow interface to RSI pin on MCC, to allow performing system reset from off-detector if necessary. Propose to implement this at half-stave/sector level for now, as it is a “safety net”. It is active-low DGND-referenced CMOS signal, and should be filtered to avoid any noise causing spurious resets.
- **NTC** and **NTC_Ret** are connected to a precision (1%) 10KΩ NTC thermistor used to monitor the module temperature (0603 part attached to Flex near module center). These signals are sent out at the module level, and are sampled by the I-box and digitized by the DCS system, both located near PP3.

Service Connections for each Module:

- **Power (3 pairs):**
- VDD/VDD_Ret, VDDA/VDDA_Ret, VDET/VDET_Ret
- **Sense (2 pairs):**
- Sense_VDD/Sense_VDD_Ret, and Sense_VDDA/Sense_VDDA_Ret
- **Temperature (1 pair):**
- NTC/NTC_Ret
- **Optical (4 pairs):**
- XCK+/-, DCI+/-, DTO+/-, DTO2+/-
- **Test (2 signals):**
- RESET (referenced to DGnd) and VCal (Vcal does not appear on Pigtail itself)
- **Comments:**
- This list includes a separate return for the NTC. This is preferred because the NTC measurement is made at PP3 in a hardware interlock, and hence needs to simple (no corrections required). The only other ground reference available at this point would be the VDET_Ret, and sharing this is not the preferred solution.
- Have also chosen to route electrical connections for two data links per module everywhere. Strictly speaking, this should be necessary only on B-layer modules.
- Sense returns are sized like supply lines due to high regulator quiescent current.

Concept for power supply connections to module:



- Ideal situation is to have the Module Common point as the only commoning point for the current flows in the regulator error amplifiers. The NTC ADC (operating in voltage excitation mode with a 2V supply) would be isolated. Both sides of the HV supply are isolated by series resistors (may need to common return line).
- Present L4913 regulator has significant current flowing in the sense return line (about 2% of load current) used to control pass transistor. In this case, coupling the sense return lines at the module and at the regulator (20-30mV voltage difference under full-load conditions) will allow current variations in one supply/ regulator to couple directly to the sensing network for the other supply/regulator.

- With separate sense return lines, there will be greater isolation between analog and digital supplies. Unfortunately, there are no SPICE models available to us for this regulator to simulate and study this, so prototype measurements will be needed. For now, strongly prefer keeping separate sense return lines for the two supplies.
- We do not like present mixing of regulator ground and sense return in L4913 design, and have discussed the possibility of implementing an improved “remote sensing” version of the L4913 with ST. This version would have a fixed quiescent current (and therefore load variations would not couple into output voltage variations in the presence of resistive sense wires).
- We are still awaiting delivery of “production” quality L4913 devices to begin serious study of regulator performance in our configuration.

Service Connections for Opto-Card

- Major concern for opto-card is reliability. Global failure on one opto-card will kill 6-7 modules. Some compromise with services plant is necessary, but no data exists on expected failure modes.
- Intend to use series resistors to partially isolate VISET for different chips. Do not believe that shorting of VVDC is likely failure mode.
- Current working design has modularity of 1 for all supplies, with all VVDC for a given opto-board connected on PP0.
- **Power (1 pair):**
- VVDC/VVDC_Ret
- **Sense (1 pair):**
- Sense_VVDC/Sense_VVDC_Ret
- **Analog Control (1 wire) referenced to VVDC_Ret:**
- VISET: voltage with 1V (1mA/DORIC) providing default VCSEL drive of 10mA.
- **Analog Power (1 pairs):**
- VPIN/VPIN_Ret
- **Temperature (1 pair):**
- NTC_OPTO/NTC_OPTO_Ret

Summary

- Presented basic electrical requirements for pixel services, based on our present best understanding of current budgets for on-detector electronics (typical and worst case).
- Introduction of 0.25μ electronics into pixel detector places stronger constraints on delivery of voltage to modules. Original large ΔV baseline with very remote control did not look adequate. Introduction of Rad-Tol regulators at PP2 looks essential, but raises reliability and stability issues that require prototyping.
- Decision on this proposal requires reliability studies, plus better understanding of grounding scheme, transient behavior of supplies/electronics, plus transient protection prototyping.
- Assumed regulator modularity of 1 per module or opto-board could allow some reduction in complex channel modularity. However, evaluation of this will require significant system testing. One of the only conservative elements of our service design is to bring individual services out as far as possible, to leave maximum flexibility for coping with grounding and noise problems.